19-1790; Rev 1; 11/05

EVALUATION KIT AVAILABLE

2.5Gbps, +3V to +5.5V, Wide Dynamic Range Transimpedance Preamplifier

General Description

The MAX3864 is a transimpedance preamplifier for applications in SDH/SONET systems operating up to 2.5Gbps. It features 490nA (typ) input-referred noise, 2.0GHz bandwidth, and 2mA input overload.

The MAX3864 operates from a single +3.0V to +5.5V supply. It includes an integrated low-frequency compensation capacitor, as well as a filter connection that provides positive bias through a 750Ω resistor to V_{CC}. These features save external components, simplifying design and assembly into a TO-46 header with a photodiode.

The MAX3864 has a typical optical dynamic range of -24dBm to 0dBm using a PIN photodetector.

Applications

SDH/SONET Transmission Systems

PIN Preamplifier Receivers

APD Preamplifier Receivers

2.5Gbps ATM Receivers

Regenerators for SDH/SONET

Features

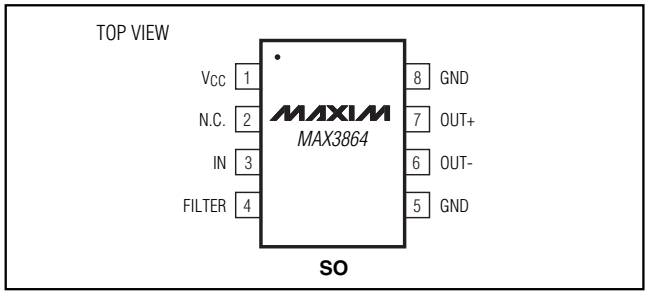
- **490nA (typ) Input-Referred Noise**
- **2000MHz Bandwidth**
- **2mA Input Overload**
- **100Ω Differential Output Impedance**
- **112mW Power Dissipation at +3.3V**
- **Integrated Filter Resistor**
- **CML Outputs**
- **Single +3.0V to +5.5V Supply Voltage**

Ordering Information

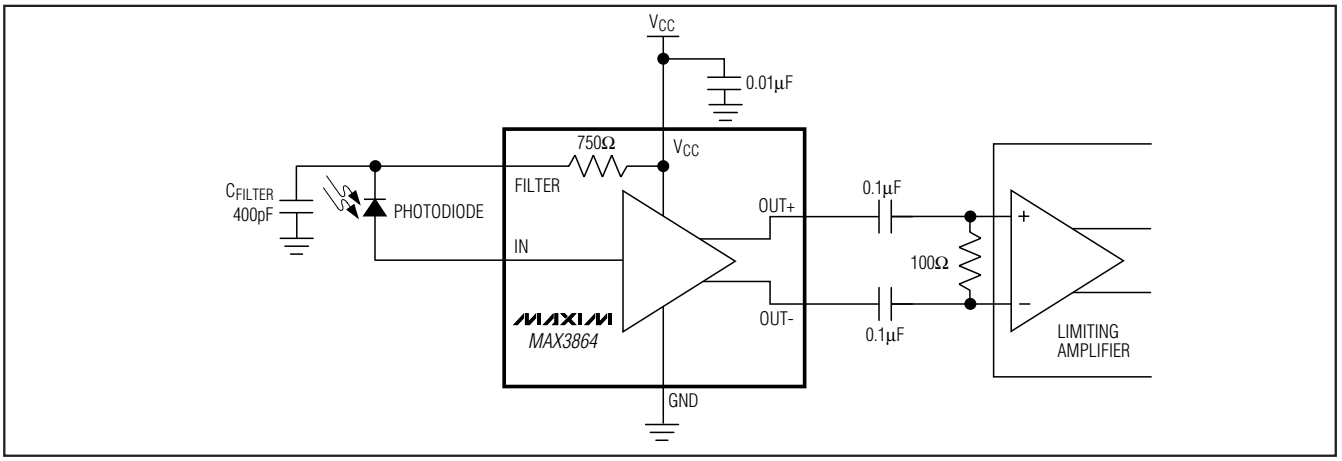
PART	TEMP RANGE	PIN-PACKAGE
MAX3864ESA	-40°C to +85°C	8 SO
MAX3864E/D	-40°C to +85°C	Dice*

** Dice are designed to operate with junction temperatures of -40°C to +140°C but are tested and guaranteed only at T_A = +25°C.*

Pin Configuration



Typical Application Circuit



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

2.5Gbps, +3V to +5.5V, Wide Dynamic Range Transimpedance Preamplifier

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} - GND) .....-0.5V to +6.0V
IN Current.....-4mA to +4mA
FILTER Current.....-8mA to +8mA
Voltages at OUT+, OUT- .....(V_{CC} - 1.5V) to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +85°C)
8-Pin SO package (derate 6.7mW/°C above +85°C) ..436mW
Storage Temperature Range .....-55°C to +150°C
Operating Junction Temperature .....-55°C to +150°C
Processing Temperature (die) .....+400°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V, 100Ω load between OUT+ and OUT-, 0.1µF coupling capacitors on OUT+ and OUT-, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at +3.3V, source capacitance = 0.85pF, and T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Bias Voltage		0.66	0.83	0.99	V
Supply Current			34	63	mA
Transimpedance	Differential, measured with 40µA_{P-P} input	2100	2750	3400	Ω
Output Impedance	Single ended (per side)	48	50	52	Ω
Maximum Differential Output Voltage	Input = 2mA_{P-P} with 100Ω differential output termination	220	380	575	mV_{P-P}
Filter Resistor		600	750	930	Ω
AC Input Overload		2			mA_{P-P}
DC Input Overload		1			mA
Input-Referred RMS Noise			490	668	nA
Input-Referred Noise Density	Bandwidth = 2.0GHz (Note 2)		11		pA/√Hz
Small-Signal Bandwidth		1525	2000		MHz
Low-Frequency Cutoff	-3dB, input ≤ 20µADC		30		kHz
Transimpedance Linear Range	Gain at 40µA_{P-P} is within 5% of the small-signal gain	40			µA_{P-P}
Deterministic Jitter	3.13V < V_{CC} < 5.5V (Note 3)		24	67	ps
	3.0V ≤ V_{CC} ≤ 3.13V (Note 3)		24	77	
Power-Supply Rejection Ratio (PSRR)	Output referred, f < 2MHz, PSRR = -20log(ΔV_{OUT}/ΔV_{CC})		50		dB

Note 1: Source capacitance represents the total capacitance at the IN pin during characterization of noise and bandwidth parameters. Noise and bandwidth will be affected by the source capacitance. See the *Typical Operating Characteristics* for more information.

Note 2: Input-referred noise is calculated as (RMS output noise) / (Gain at f = 10MHz). Noise density is (Input-Referred Noise) / (Bandwidth)$^{1/2}$. No external filters are used for the noise measurements.

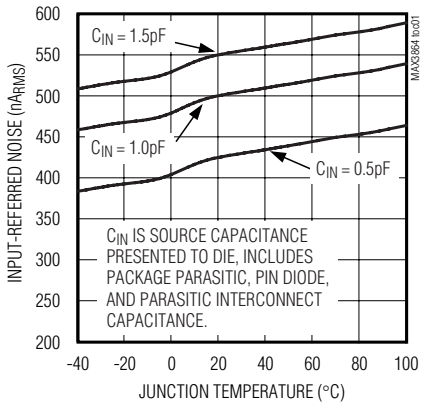
Note 3: Deterministic jitter is defined as the arithmetic sum of pulse-width distortion and pattern dependent jitter measured with a repeating 20-bit pattern of 00111110101100000101 (K28.5). See *Typical Operating Characteristics*.

2.5Gbps, +3V to +5.5V, Wide Dynamic Range Transimpedance Preamplifier

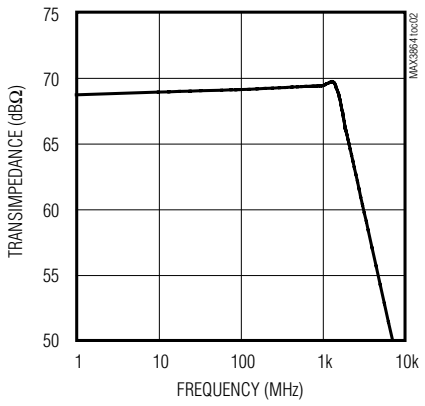
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C and MAX3864 EV kit source capacitance = 0.85pF, unless otherwise noted).

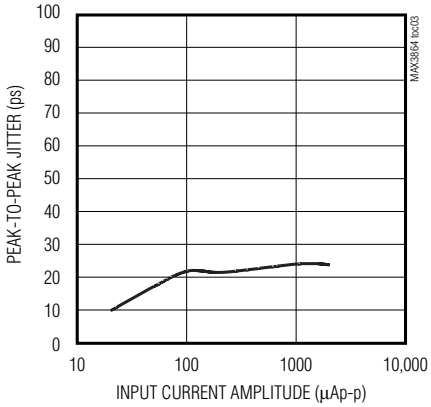
INPUT-REFERRED RMS NOISE vs. TEMPERATURE



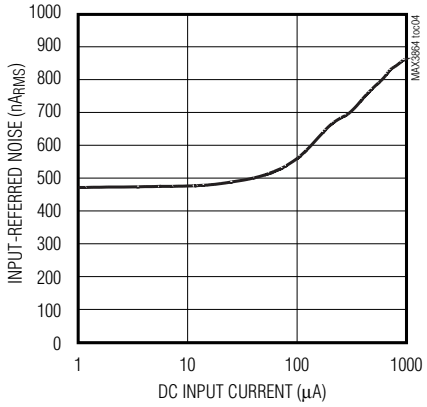
FREQUENCY RESPONSE



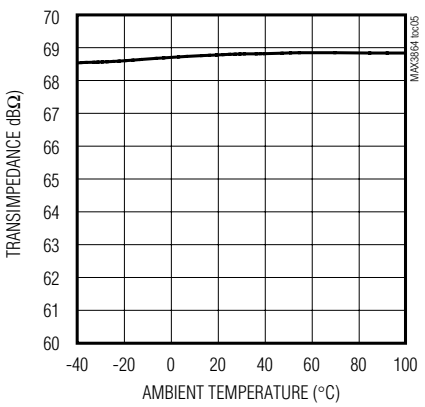
DETERMINISTIC JITTER vs. INPUT AMPLITUDE



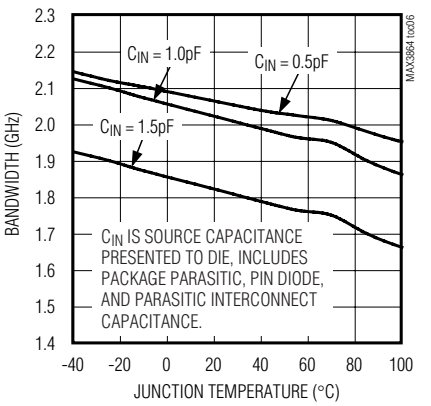
INPUT-REFERRED RMS NOISE CURRENT vs. DC INPUT CURRENT



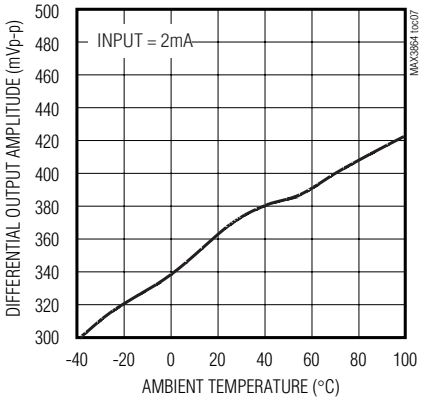
SMALL-SIGNAL TRANSIMPEDANCE vs. TEMPERATURE



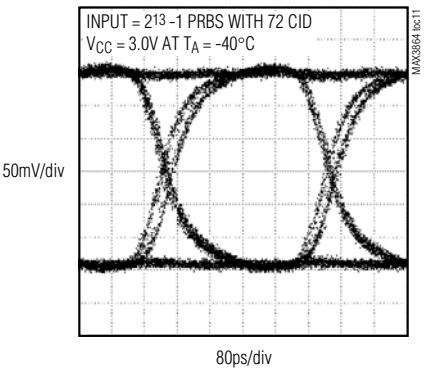
BANDWIDTH vs. TEMPERATURE



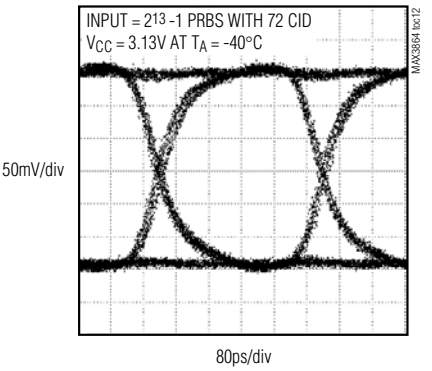
DIFFERENTIAL OUTPUT AMPLITUDE vs. TEMPERATURE



EYE DIAGRAM (INPUT = 2mAP-P)



EYE DIAGRAM (INPUT = 2mAP-P)

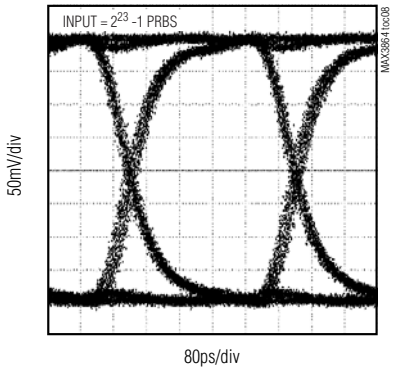


2.5Gbps, +3V to +5.5V, Wide Dynamic Range Transimpedance Preamplifier

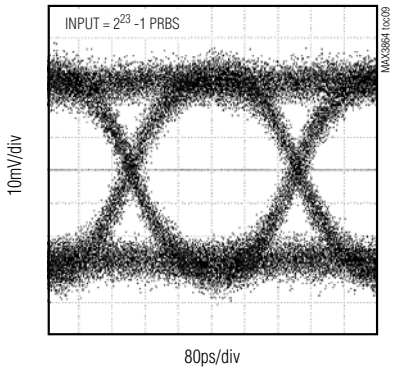
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C and MAX3864 EV kit source capacitance = 0.85pF, unless otherwise noted).

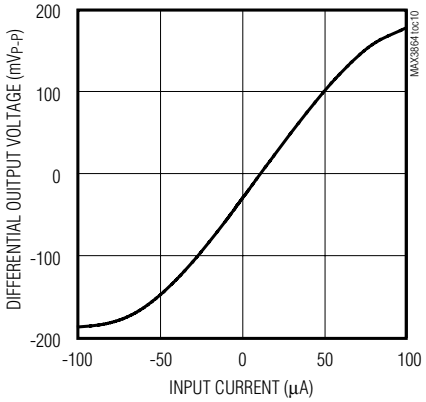
EYE DIAGRAM (INPUT = 2mA$_{P-P}$)



EYE DIAGRAM (INPUT = 20µA$_{P-P}$)



DC TRANSFER FUNCTION



Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Supply Voltage
2	N.C.	No Connection
3	IN	Amplifier Input
4	FILTER	Provides bias voltage for the photodiode through a 750Ω resistor to V_{CC}. When grounded, this pin disables the DC cancellation amplifier to allow a DC path from IN to OUT+ and OUT- for testing.
5	GND	Ground
6	OUT-	Inverting Output. Current flowing into IN causes V_{OUT-} to decrease.
7	OUT+	Noninverting Output. Current flowing into IN causes V_{OUT+} to increase.
8	GND	Ground

Detailed Description

The MAX3864 transimpedance amplifier is designed for 2.5Gbps fiber optic applications. As shown in Figure 1, the MAX3864 comprises a transimpedance amplifier, a voltage amplifier, an output buffer, an output filter, and a DC cancellation circuit.

Transimpedance Amplifier

The signal current at the input flows into the summing node of a high-gain amplifier. Shunt feedback through R_F converts this current to a voltage. Schottky diodes clamp the output voltage for large input currents (Figure 2).

Voltage Amplifier

The voltage amplifier converts single-ended signals to differential signals and introduces a voltage gain.

Output Buffer

The output buffer provides a back-terminated voltage output. The buffer is designed to drive a 100Ω differential load between OUT+ and OUT-. The output voltage is divided between internal 50Ω load resistors and the external load resistor. In the typical operating circuit, this creates a voltage-divider with a ratio of 1/2. The MAX3864 can also be terminated with higher output impedances, which increases gain and output voltage swings.

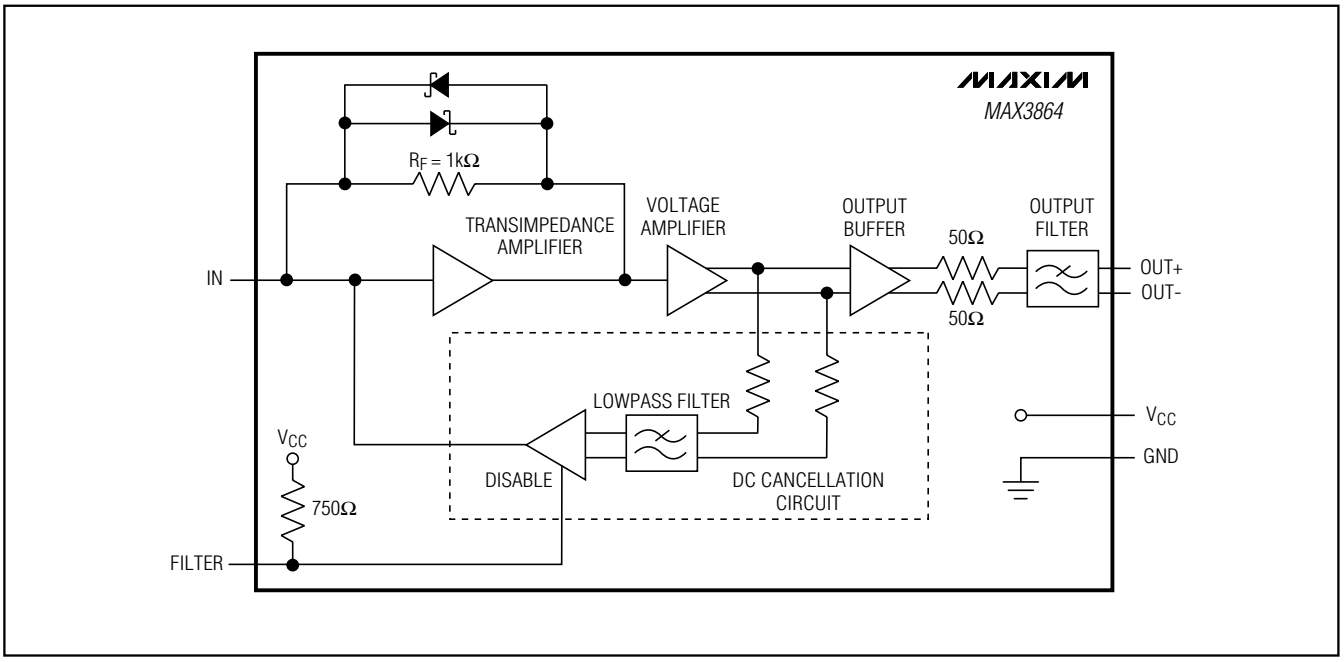


Figure 1. Functional Diagram

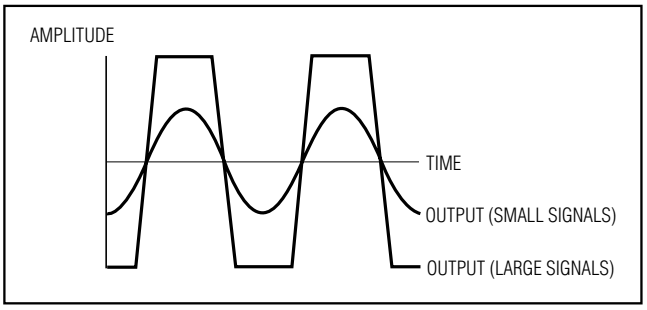


Figure 2. Limited Output

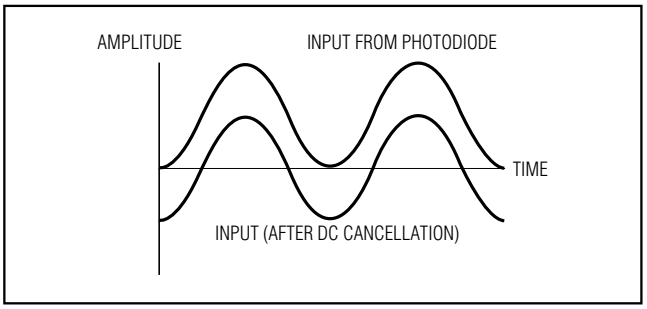


Figure 3. DC Cancellation Effect on Input

For optimum supply-noise rejection, the MAX3864 should be terminated with a differential load. If a single-ended output is required, the unused output should be terminated with 50Ω to V_{CC}. The MAX3864 will not drive a DC-coupled, 50Ω grounded load.

Output Filter

The MAX3864 includes a one-pole lowpass filter that limits the circuit bandwidth and improves noise performance.

DC Cancellation Circuit

The DC cancellation circuit uses low-frequency feedback to remove the DC component of the input signal (Figure 3). This feature centers the input signal within the transimpedance amplifier's linear range, thereby reducing pulse-width distortion (PWD) on large input signals.

The DC cancellation circuit is internally compensated and therefore does not require external capacitors. This circuit minimizes PWD for data sequences that exhibit a 50% duty cycle and mark density. A duty cycle or mark density significantly different from 50% causes the MAX3864 to generate PWD.

DC cancellation current is drawn from the input and creates noise. For low-level signals with little or no DC component, this is not a problem. Amplifier noise will increase for signals with significant DC component (see *Typical Operating Characteristics*).

2.5Gbps, +3V to +5.5V, Wide Dynamic Range Transimpedance Preamplifier

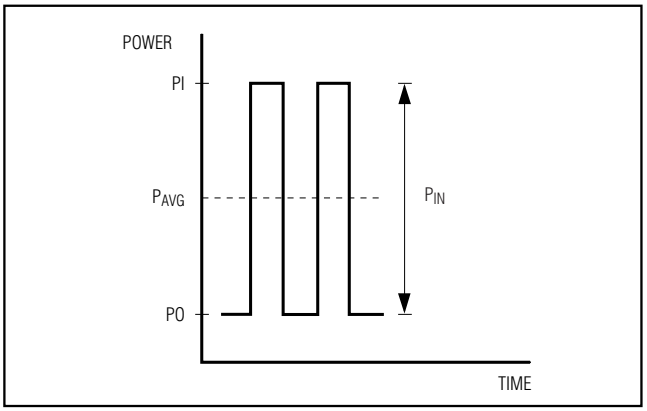


Figure 4. Optical Power Relations

Table 1. Optical Power Relations

PARAMETER	SYMBOL	RELATION
Average Power	P_{AVE}	$P_{AVE} = (P_0 + P_1) / 2$
Extinction Ratio	r_e	$r_e = P_1 / P_0$
Optical Power of a 1	P_1	$P_1 = 2P_{AVE}r_e / (r_e + 1)$
Optical Power of a 0	P_0	$P_0 = 2P_{AVE} / (r_e + 1)$
Signal Amplitude	P_{IN}	$P_{IN} = P_1 - P_0 = 2P_{AVE} (r_e - 1) / (r_e + 1)$

Note: *Assuming a 50% average input duty cycle and mark density.*

Applications Information

Optical Power Relations

Many of the MAX3864 specifications relate to the input signal amplitude. When working with fiber optic receivers, the input is usually expressed in terms of average optical power and extinction ratio. Figure 4 shows relations that are helpful for converting optical power to input signal when designing with the MAX3864.

Optical power relations are shown in Table 1; the definitions are true if the average duty cycle and mark density of the input data are 50%.

Optical Sensitivity Calculations

The MAX3864 input-referred RMS noise current (I_N) generally determines the receiver sensitivity. To obtain a system bit-error rate (BER) of 1E-10, the minimum signal-to-noise ratio (SNR) is 12.7. The input sensitivity, expressed in average power, can be estimated as:

$$\text{Sensitivity} = 10\log\left(\frac{\text{SNR} \times I_N(r_e + 1)}{2\rho(r_e - 1) \times 1000}\right) \text{dBm}$$

where ρ is the photodiode responsivity, including fiber-to-photodiode coupling efficiency in A/W and I_N in µA. For example, if SNR = 12.7, I_N = 0.490µA, r_e = 10, and ρ = 1, then sensitivity is -24dBm.

Input Optical Overload

The overload is the largest input that the MAX3864 accepts while meeting deterministic jitter specifications. The optical overload can be estimated in terms of average power with the following equation (assumes $r_e = \infty$):

$$\text{Overload} = 10\log\left(\frac{2\text{mAp-p} \times 1000}{2\rho}\right) \text{dBm}$$

Optical Linear Range

The MAX3864 has high gain, which limits the outputs when the input signal exceeds 40µA$_{P-P}$. The MAX3864 operates in a linear range for inputs not exceeding:

$$\text{Linear Range} = 10\log\left(\frac{40\mu\text{Ap-p}(r_e + 1) \times 1000}{2\rho(r_e - 1)}\right) \text{dBm}$$

Layout Considerations

Use good high-frequency design and layout techniques. The use of a multilayer circuit board with separate ground and power planes is recommended. Connect the GND pins to the ground plane with the shortest possible traces.

Noise performance and bandwidth will be adversely affected by capacitance at the IN pin. Minimize capacitance on this pin, and select a low-capacitance photodiode. Assembling the MAX3864 in die form using chip and wire technology provides the best possible performance. Figure 5 shows the recommended layout for a TO header.

The SO package version of the MAX3864 is offered as an easy way to characterize the circuit and to become familiar with the circuit's operation, but it does not offer optimum performance. When using the SO version of the MAX3864, the package capacitance adds approximately 0.3pF at the input. The PC board between the MAX3864 input and the photodiode also adds parasitic capacitance. Keep the input line short, and remove power and ground planes beneath it.

GND

Connect GND as close to the AC ground of the photodetector diode as possible. The photodetector AC ground is usually the ground of the filter capacitor from the photodetector cathode. The total loop (from GND, through the bypass capacitor and the diode, and back to IN) should be no more than approximately 1/5th of a wavelength.

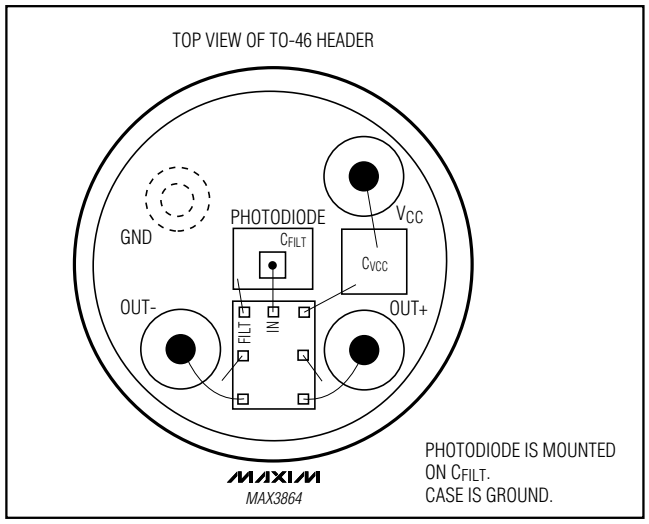


Figure 5. Suggested Layout for TO-46 Header

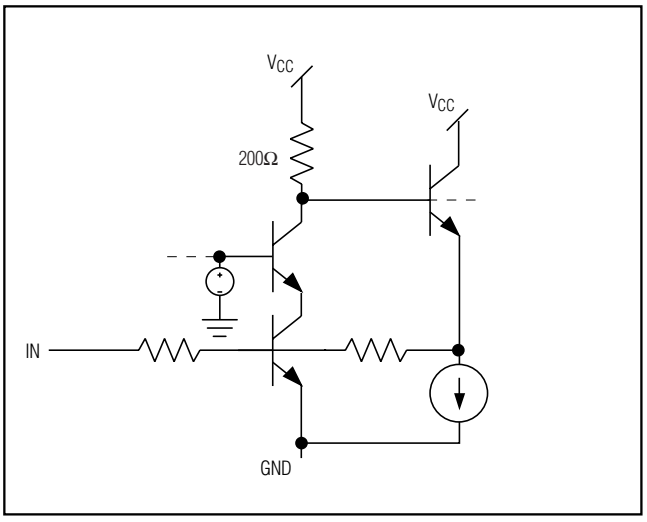


Figure 6. Equivalent Input Circuit

Photodiode Filter

Supply voltage noise at the photodiode cathode produces a current $I = C_{PD} \Delta V / \Delta t$, which reduces the receiver sensitivity (C_{PD} is the photodiode capacitance). The filter resistor of the MAX3864, combined with an external capacitor, can be used to reduce this noise (see the *Typical Application Circuit*). Current generated by supply noise voltage is divided between C_{FILTER} and C_{PD}. The input noise current due to supply noise is (assuming the filter capacitor is much larger than the photodiode capacitance):

$$I_{NOISE} = \frac{\left(V_{NOISE}\right)\left(C_{PD}\right)}{\left(R_{FILTER}\right)\left(C_{FILTER}\right)}$$

If the amount of tolerable noise is known, the filter capacitor can be easily selected:

$$C_{FILTER} = \frac{\left(V_{NOISE}\right)\left(C_{PD}\right)}{\left(R_{FILTER}\right)\left(I_{NOISE}\right)}$$

For example, with a maximum noise voltage equal to $100mV_{P-P}$, C_{PD} = 0.85pF, R_{FILTER} = 750Ω, and I_{NOISE} selected to be 250nA (half of the MAX3864's input noise):

$$C_{FILTER} = \frac{\left(100mV\right)\left(0.85pF\right)}{\left(750\Omega\right)\left(250nA\right)} = 453pF$$

Wire Bonding

For high current density and reliable operation, the MAX3864 uses gold metalization. Connections to the die should be made with gold wire only, using ball-bonding. Wedge bonding is not recommended. Die thickness is typically 15mils (0.375mm).

2.5Gbps, +3V to +5.5V, Wide Dynamic Range Transimpedance Preamplifier

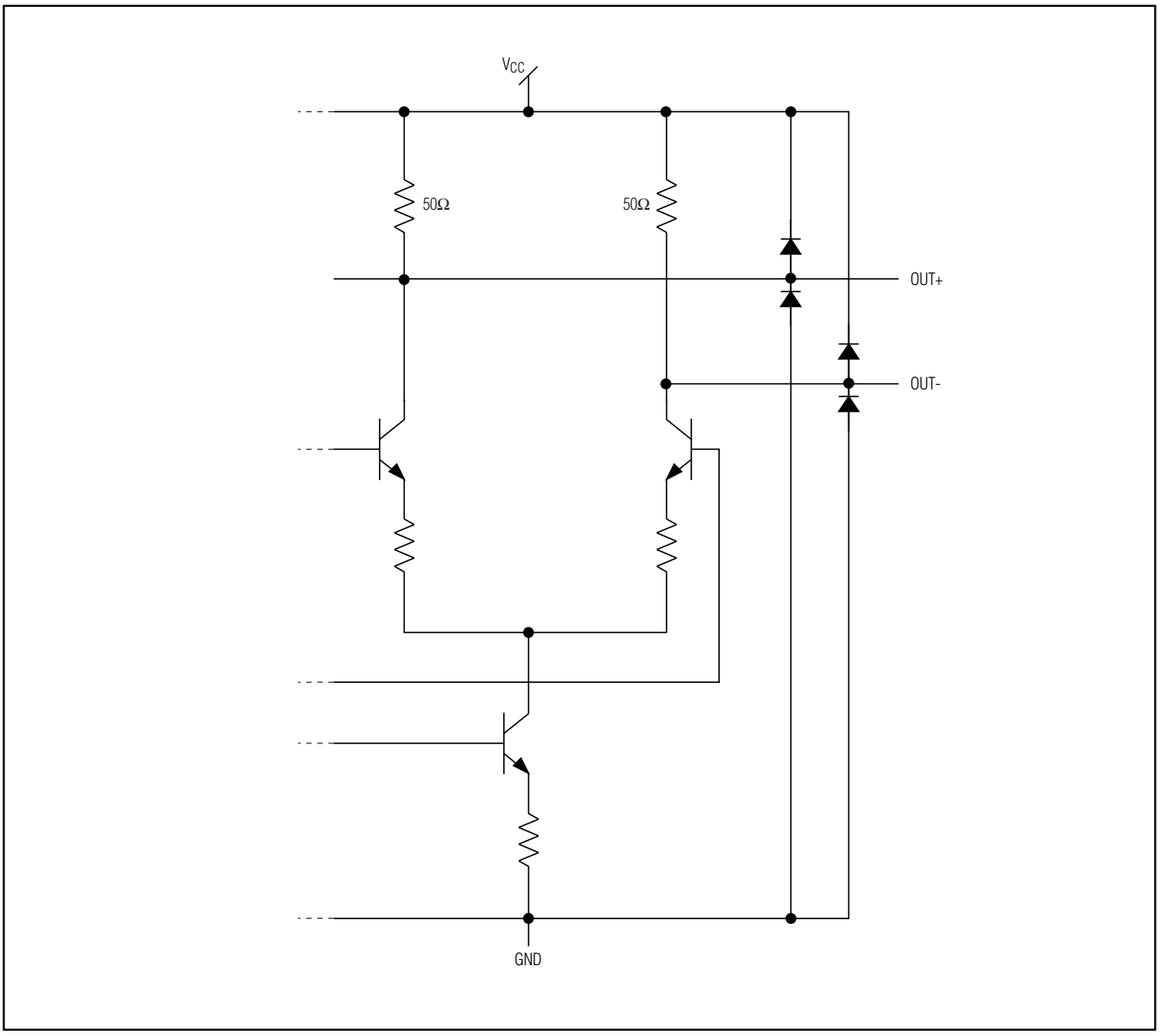
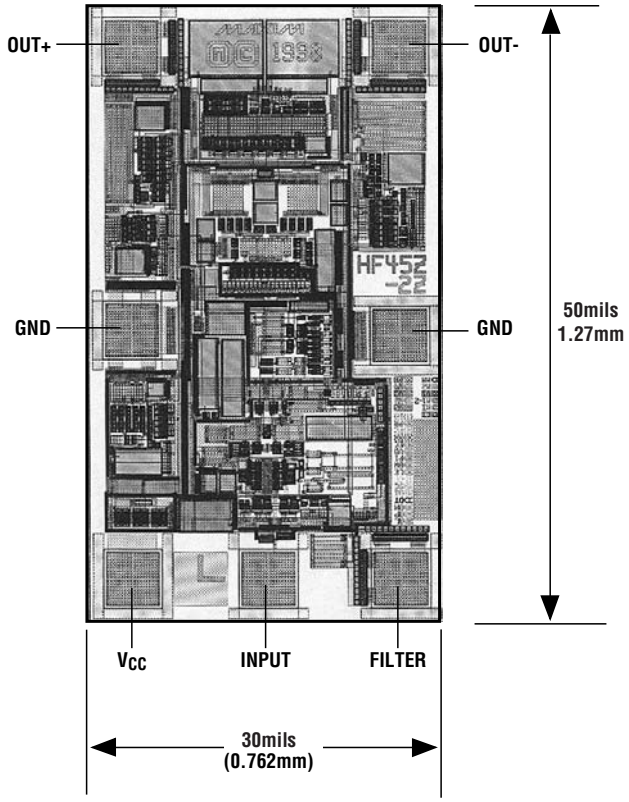


Figure 7. Equivalent Output Circuit

2.5Gbps, +3V to +5.5V, Wide Dynamic Range Transimpedance Preamplifier

Chip Topography



Chip Information

TRANSISTOR COUNT: 320

PROCESS: BIPOLAR (SILICON GERMANIUM)

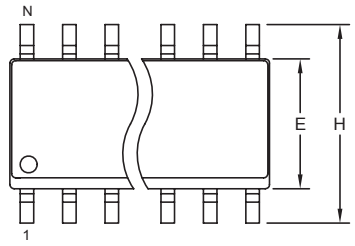
2.5Gbps, +3V to +5.5V, Wide Dynamic Range Transimpedance Preamplifier

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOICN .EPS

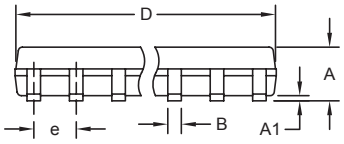
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27



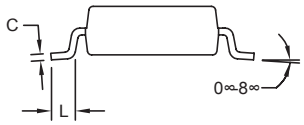
TOP VIEW

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

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